ABSTRACT

A new method of forming shallow trench isolations has been described. A silicon semiconductor substrate is provided. A silicon nitride layer is deposited overlying the substrate. A polysilicon layer is deposited overlying the silicon nitride layer. An oxidation mask is deposited overlying the polysilicon layer. The oxidation mask, polysilicon layer, silicon nitride layer, and the silicon semiconductor substrate are patterned to form trenches for planned shallow trench isolations. The silicon semiconductor substrate exposed within the trenches is oxidized to form an oxide liner layer within the trenches wherein the oxidation mask prevents oxidation of the polysilicon layer. Thereafter the oxidation mask is removed. A trench oxide layer is deposited overlying the liner oxide layer and filling the trenches. The trench oxide layer and the polysilicon layer are polished down stopping at the silicon nitride layer with a polishing selectivity of oxide to polysilicon to nitride of 4:100:1 wherein dishing is avoided to complete shallow trench isolations in the manufacture of an integrated circuit device.